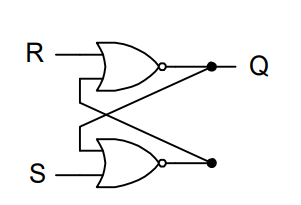
*Project by:*

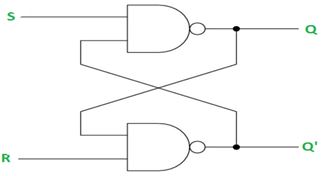
*Mohannad Wael Taman 19100213 Mohammed Nasser El-Maghraby 19102722 Class C*

SR Latch

The SR-latch is shown below utilizing 2-NOR gates with a cross loop connection.

These latches can be also built with NAND gates

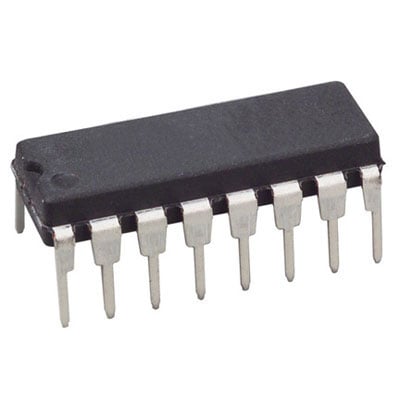


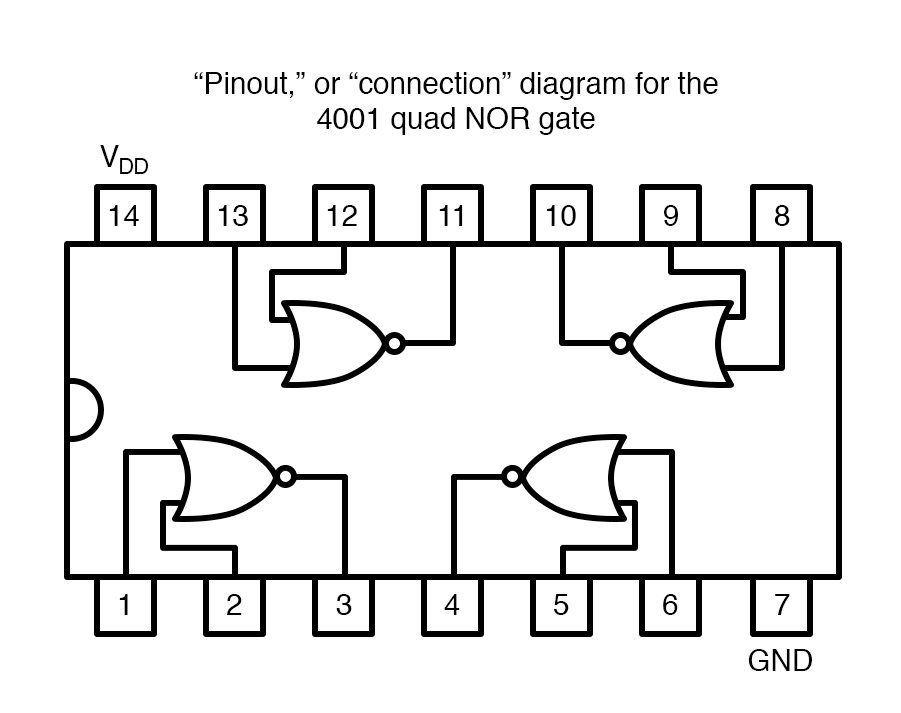


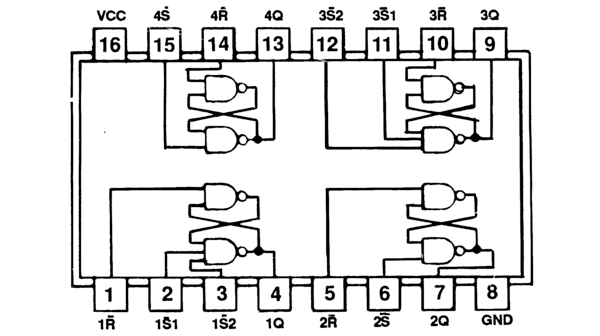
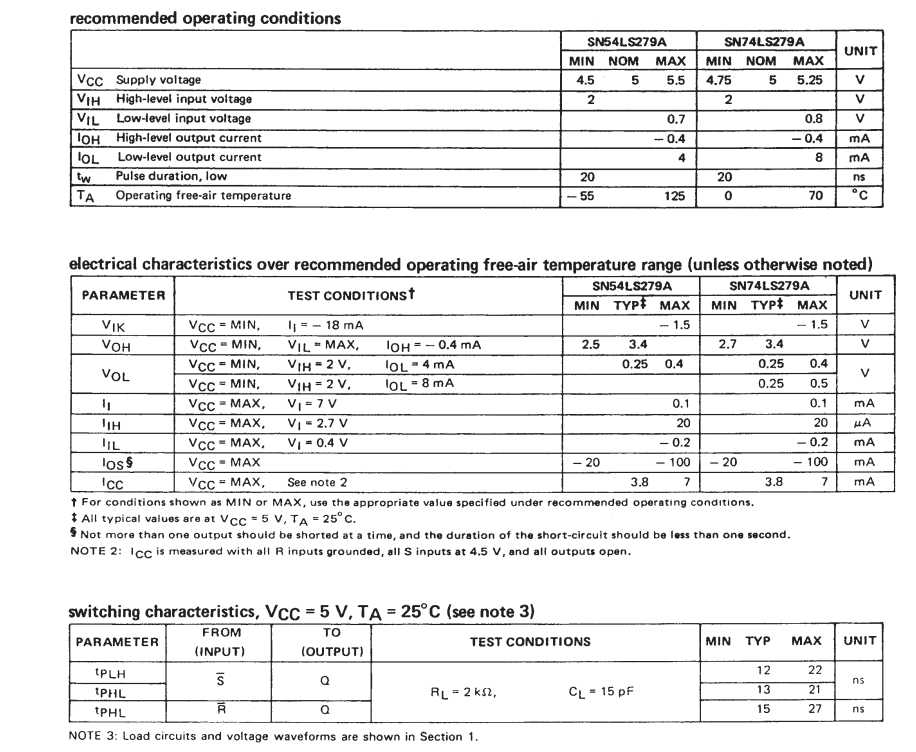
latch is a type of logic circuit in digital electronics that is also known as a bistable-multivibrator. Because it can exist in two stable states: active high and active low. It functions as a storage device by storing data in a feedback lane. As long as the Power device is turned on, it stores one piece of data. When enable is declared, latch can modify the stored data immediately.

An SR latch (Set/Reset) is an asynchronous device: it works independently of control signals and relies only on the state of the S and R inputs, Therefore it doesn’t depend on the CLK it changes its whe there is a change in The SR inputs

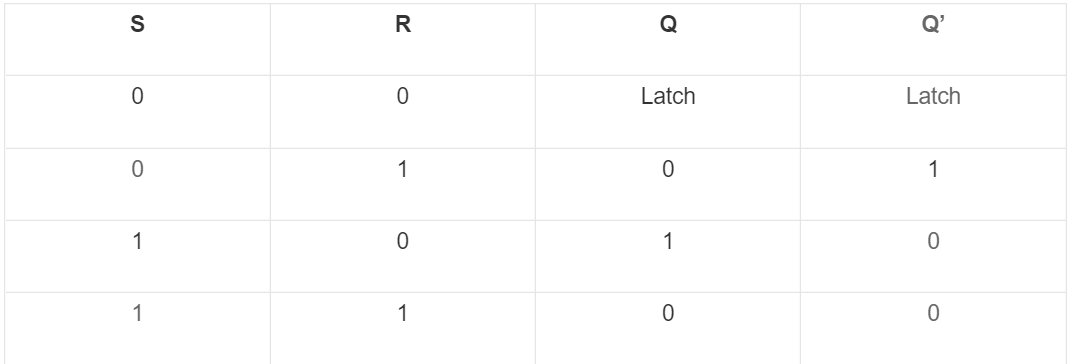
IC







Truth Table



When the S-line of the latch receives a high input, the output Q also becomes high. When the S-input becomes low again in the feedback process, the output Q will remain high. The latch functions as a memory device in this fashion.

Q will always have the value as S

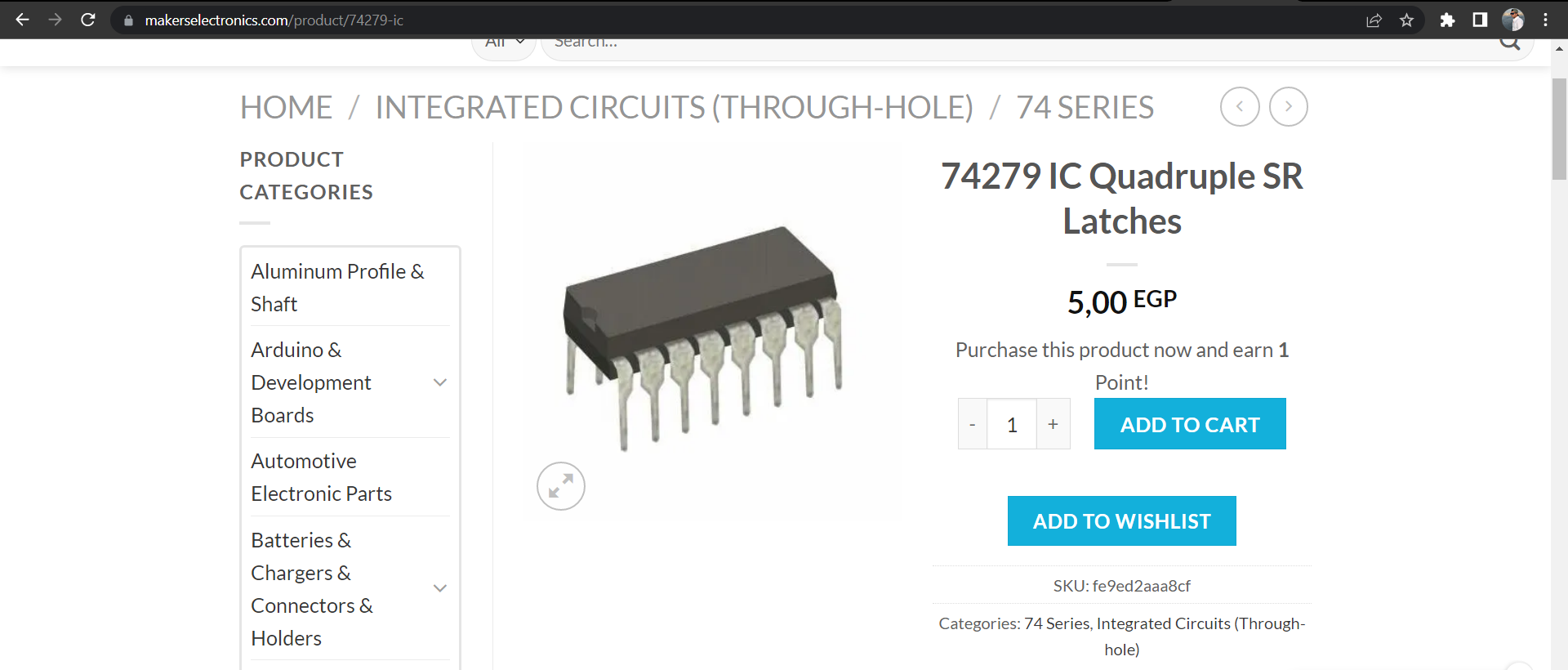
Qbar will always have the value of the R

In case you didn’t Set or Reset ( 0 and 0 ) Q and Qbar will remain unchanged “Memory”

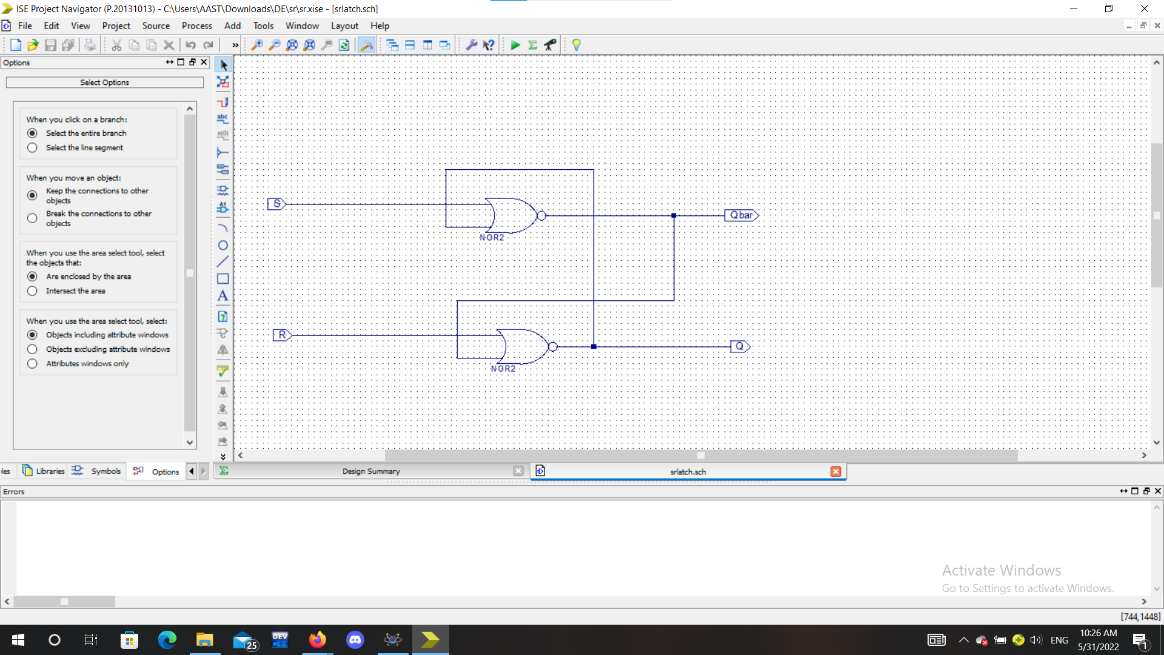
Case of both Set and Reset are both high is an invalid case as it is only allowed to Set or Reset at once

Because when both inputs are high at the same time, there's a problem: it's being commanded to generate a high Q and a low Q at the same time. This creates a race condition in the circuit since whichever flip flop changes first will respond to the other and announce itself. Both logic gates should be equal, and the gadget should be in an indeterminate state for an extended period of time.

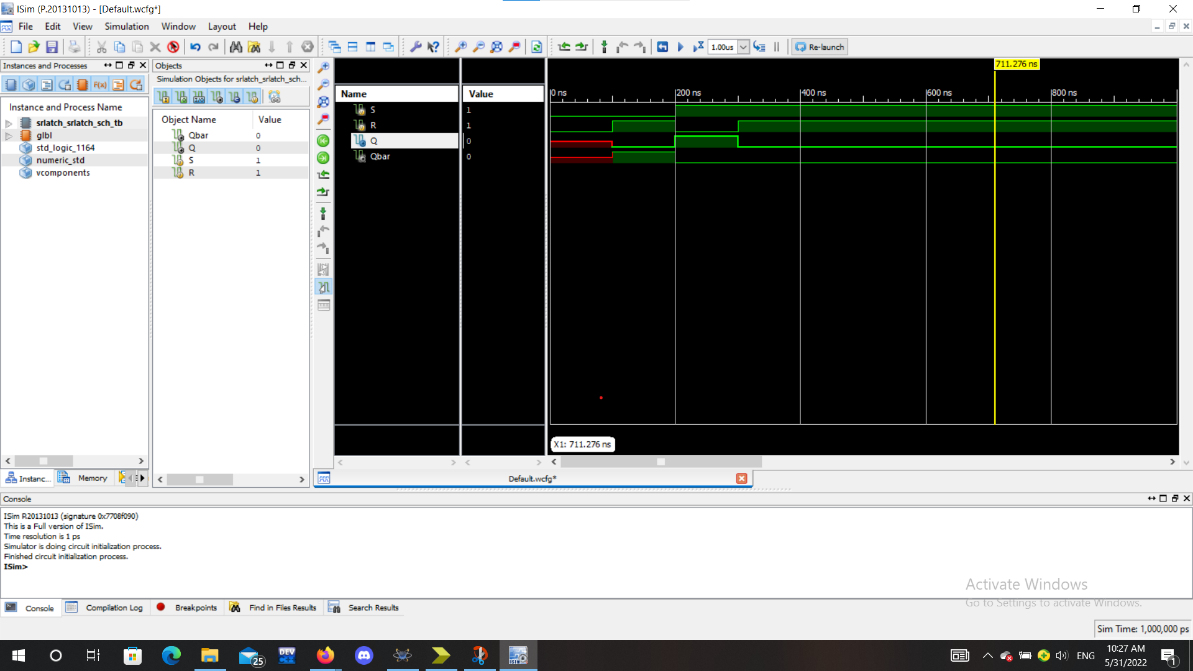
Market Value



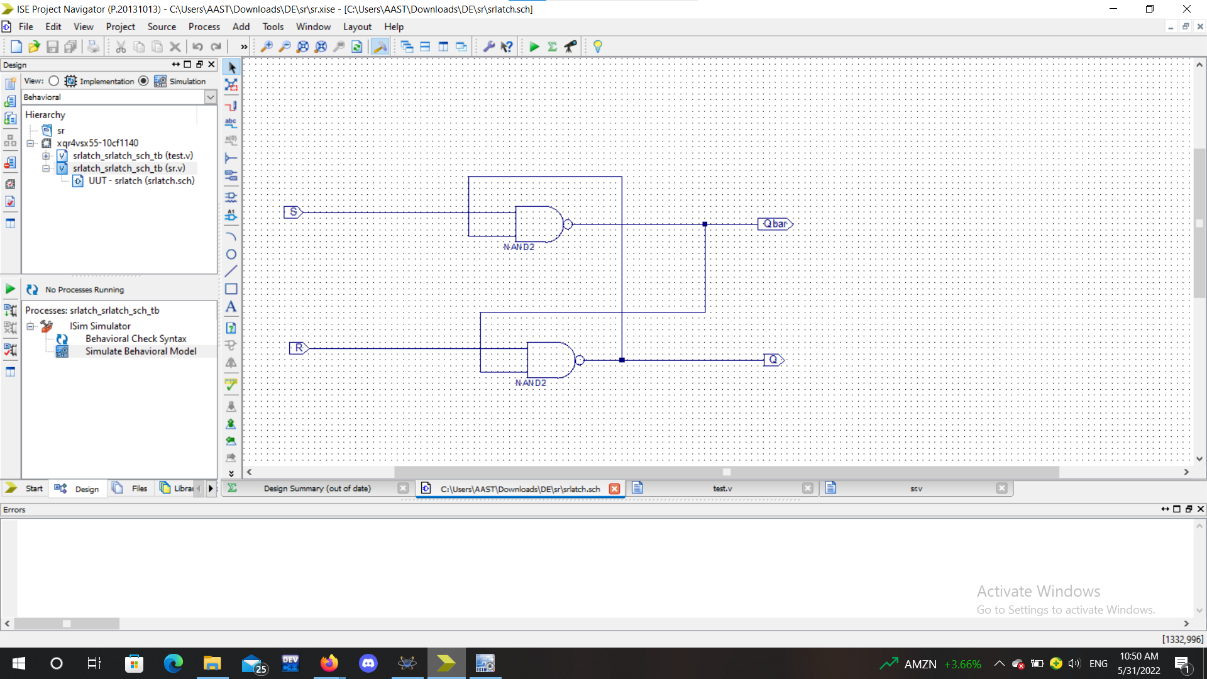
Simulation

SR LATCH USING NOR IMPLEMENTATION:

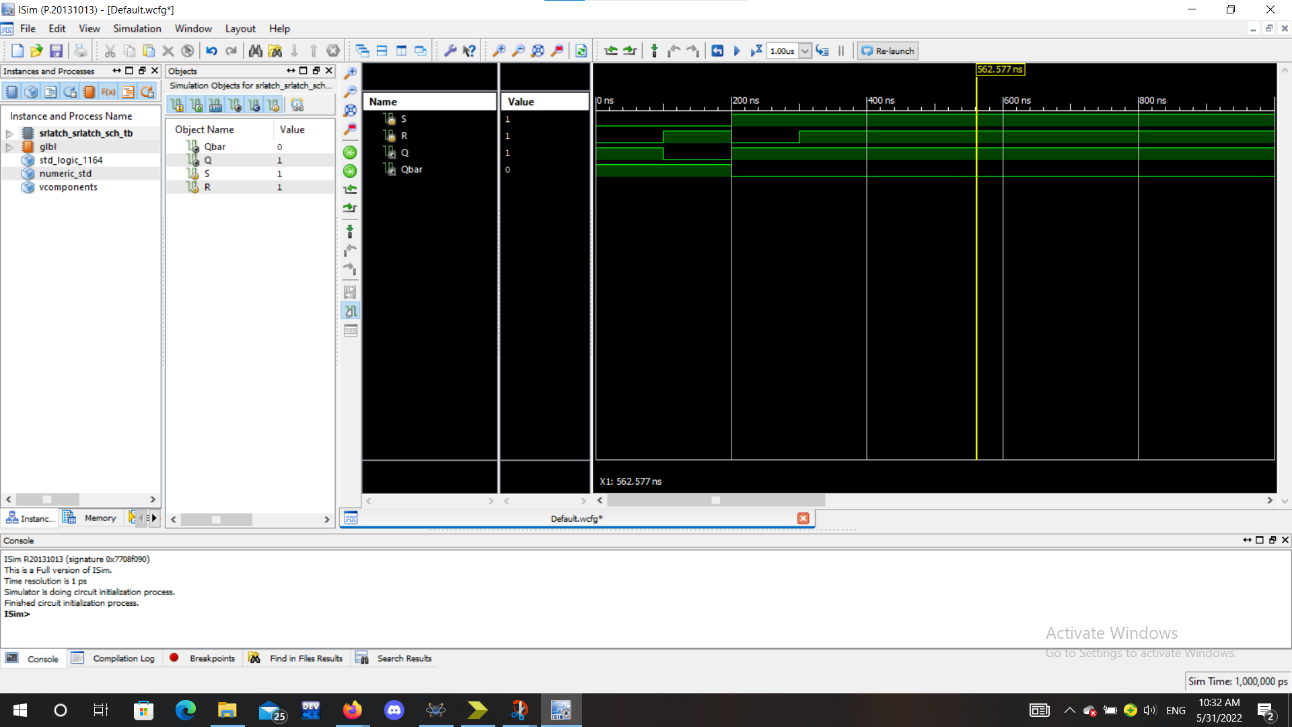
SR LATCH USING NOR SIMULATION:



SR LATCH USING NAND IMPLEMENTATION:

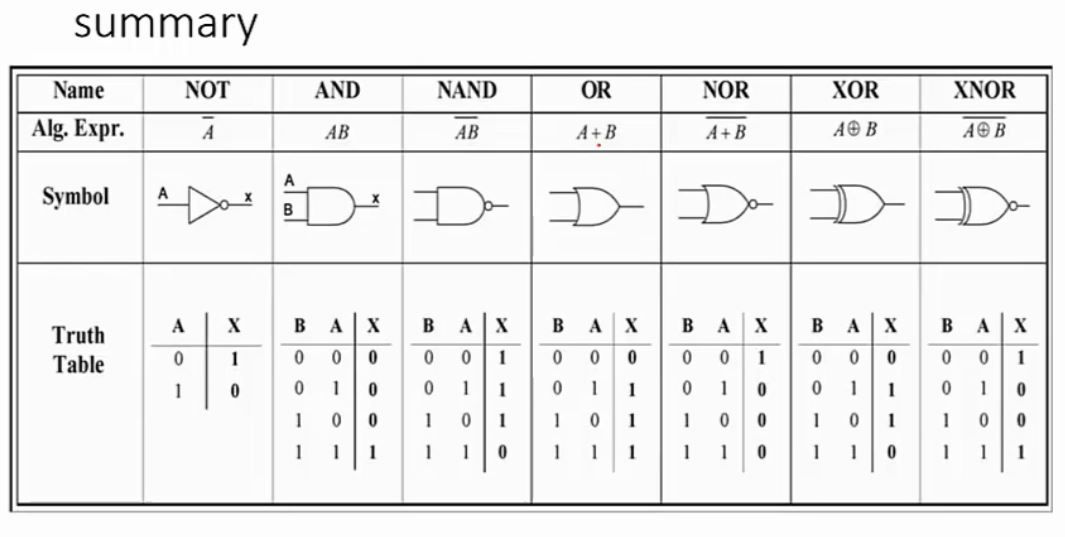


SR LATCH USING NAND SIMULATION:

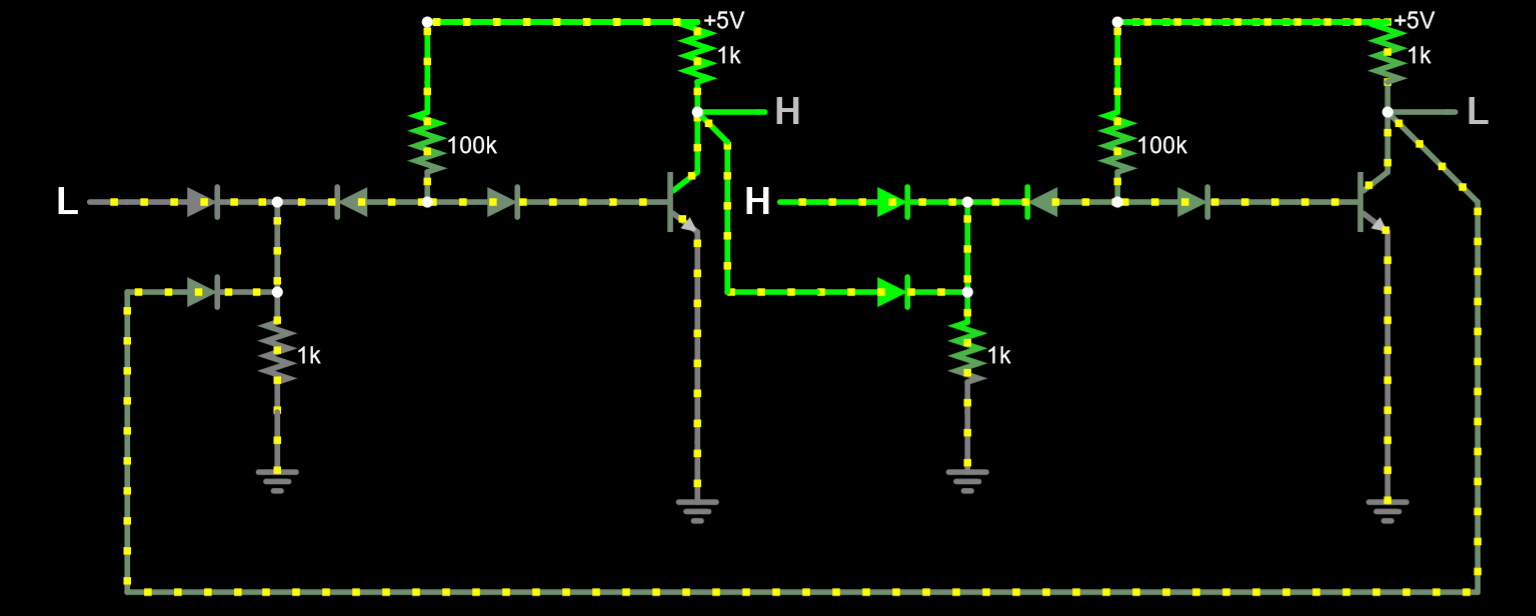


SR Latches can be implemented in various ways as mentioned above

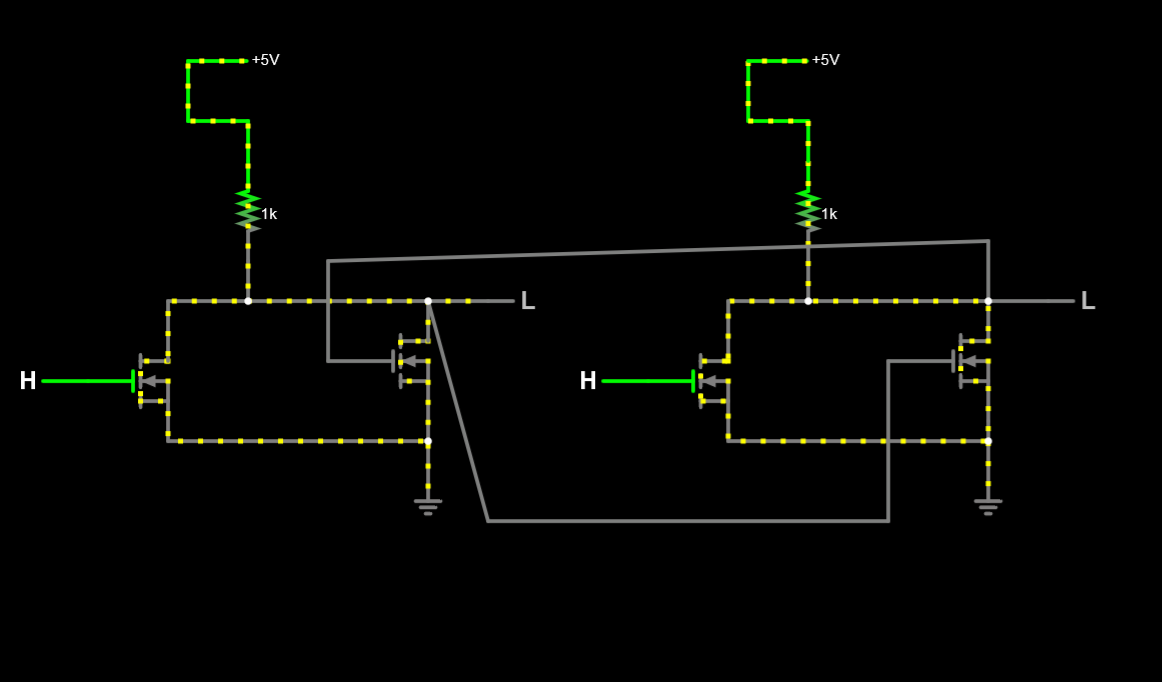
Not only SR Latches that can be implemented in various ways, but alos Logic Gates can be implements using different components and methods, each with its own advantages and disadvantages

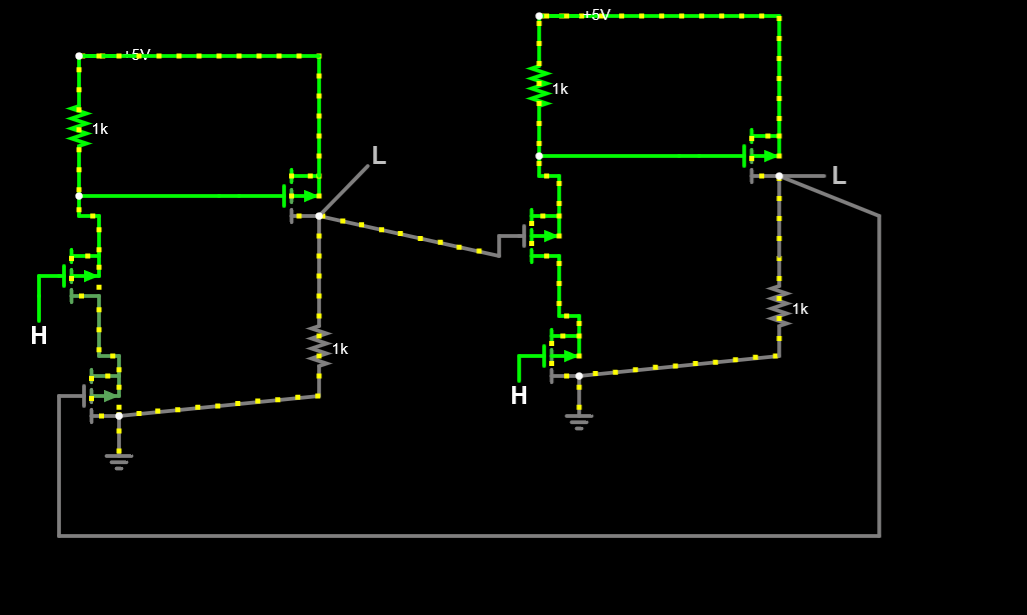


SR LATCH USING DTL:

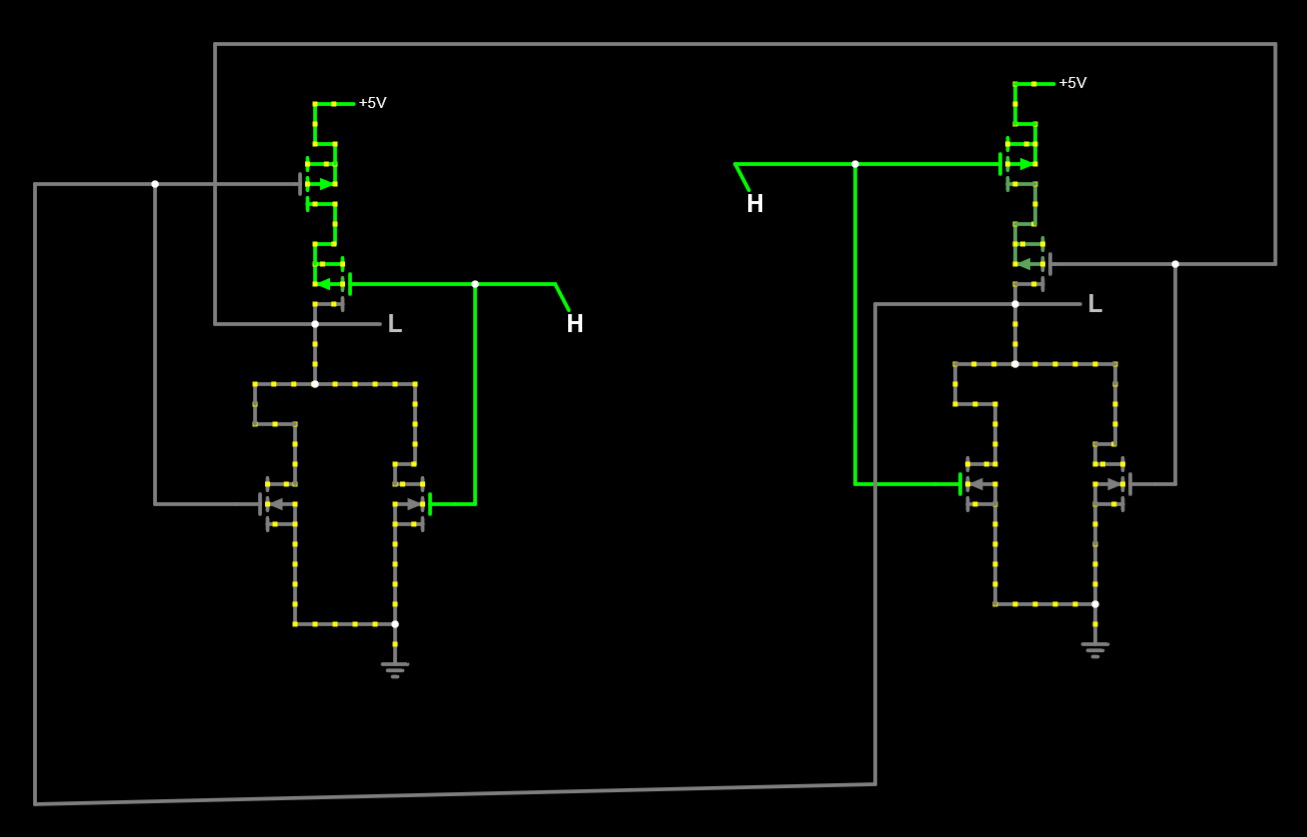


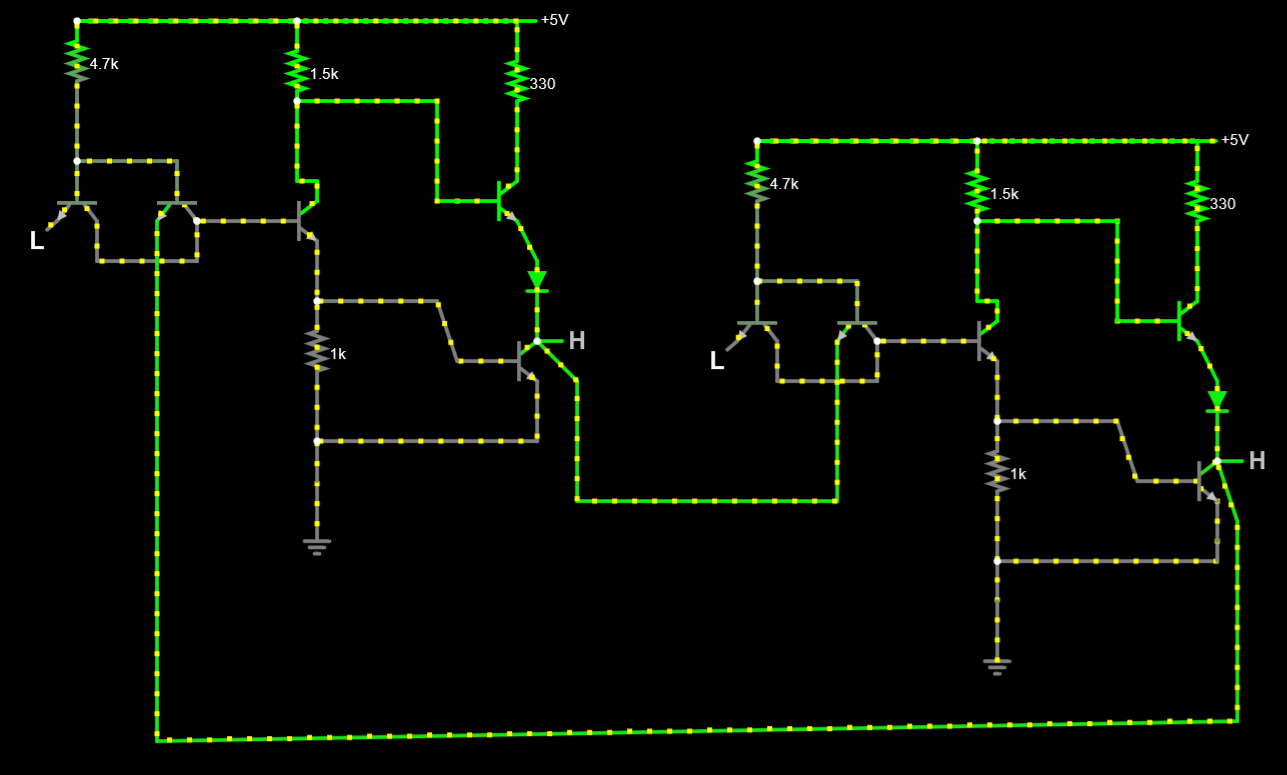
SR LATCH USING NMOS:



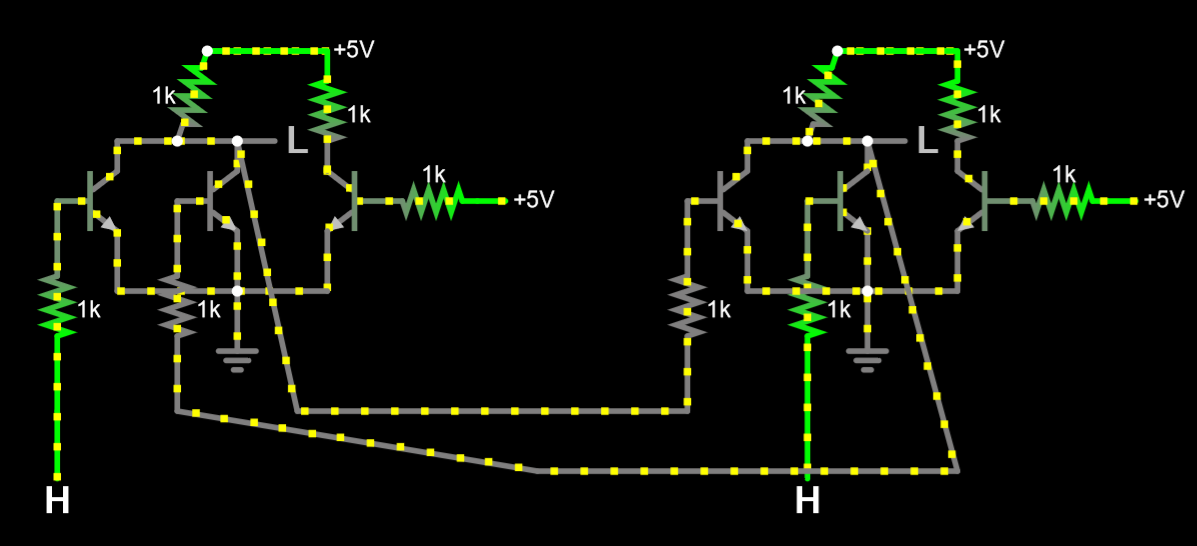
SR LATCH USING PMOS:

SR LATCH USING CMOS:



SR LATCH USING TTL:

SR LATCH USING ECL:



Poster

